

one or more vertical routing channels;

5           one or more logic elements each configured to (i) receive  
one or more inputs from one of said horizontal routing channels and  
one of said vertical routing channels and (ii) present one or more  
outputs to said horizontal routing channel and said vertical  
routing channel, wherein each of said logic elements comprises (i)  
10   a logic block array and (ii) an interconnect matrix coupled to said  
logic block array, said horizontal routing channel and said  
vertical routing channel; and

          a memory block configured to (i) receive one or more  
inputs from and (ii) present one or more outputs to either (a) said  
15   interconnect matrix or (b) said horizontal routing channel and said  
vertical routing channel.

2.   (PREVIOUSLY AMENDED) The programmable logic device  
according to claim 1, wherein said memory block comprises a first  
port connected to one of said horizontal routing channels and a  
second port connected to one of said vertical routing channels.

3.   The programmable logic device according to claim 2,  
wherein said memory block is configured as a synchronous dual port  
memory.

4. The programmable logic device according to claim 2, wherein said memory block is configured as an asynchronous dual port memory.

5. The programmable logic device according to claim 2, wherein said memory block is configured as a synchronous FIFO memory.

6. (PREVIOUSLY AMENDED) The programmable logic device of claim 1, wherein said memory block is coupled to said interconnect matrix.

7. The programmable logic device of claim 1, further comprising a plurality of I/O blocks, wherein each I/O block of said plurality of I/O blocks is connected to a different end of said horizontal and said vertical routing channels.

8. The programmable logic device of claim 7, wherein said I/O blocks are grouped into I/O banks.

9. The programmable logic device of claim 7, wherein said I/O blocks comprise configurable I/O cells.

10. The programmable logic device of claim 1, further comprising one or more dedicated inputs for I/O cell control.

11. The programmable logic device of claim 1, further comprising one or more dedicated clock inputs.

12. The programmable logic device of claim 11, further comprising a phase lock loop circuit configured to generate one or more global clock signals in response to one or more input clock signals.

13. The programmable logic device of claim 10, wherein said dedicated inputs for I/O control comprise a reset input.

14. The programmable logic device of claim 10, wherein said dedicated inputs for I/O control comprise an output enable input.

15. The programmable logic device of claim 10, wherein said dedicated inputs for I/O control comprise a clock enable input.

16. The programmable logic device of claim 11, further comprising a phase lock loop circuit configured to generate one or

more global clock signals by multiplying or dividing a frequency of a clock signal presented to said one or more dedicated clock inputs.

17. (PREVIOUSLY ADDED) The programmable logic device of claim 1, wherein said logic block array comprises a plurality of logic blocks.

18. (PREVIOUSLY ADDED) The programmable logic device of claim 17, wherein each logic block of said logic block array comprises a product term array configured to receive inputs from said interconnect matrix.

19. (PREVIOUSLY ADDED) The programmable logic device of claim 18, wherein each of said logic blocks further comprise a plurality of macrocells each having an output coupled to said interconnect matrix.

20. (PREVIOUSLY ADDED) The programmable logic device of claim 19, wherein each of said logic blocks further comprises an OR array coupling said product term array to said plurality of macrocells.

21. (PREVIOUSLY ADDED) The programmable logic device of claim 1, wherein said interconnect matrix comprises a programmable interconnect matrix.

22. (PREVIOUSLY ADDED) The programmable logic device of claim 6, wherein said interconnect matrix couples said memory block to one of said horizontal routing channels, one of said vertical routing channels, and said logic block array.

23. (PREVIOUSLY ADDED) The programmable logic device of claim 1, comprising a plurality of horizontal routing channels and a plurality of vertical routing channels.

24. (PREVIOUSLY ADDED) The programmable logic device of claim 1, comprising a plurality of logic elements.

25. (PREVIOUSLY ADDED) The programmable logic device of claim 23, comprising at least four logic elements.

26. (AMENDED) A programmable logic device comprising:

a plurality of horizontal routing channels;

a plurality of vertical routing channels;

a plurality of first memory blocks; and

5 a plurality of logic block arrays, wherein each of said plurality of first memory blocks and each of said plurality of logic block arrays is configured to (i) receive one or more inputs from one of said plurality of horizontal routing channels and one of said plurality of vertical routing channels and (ii) present one  
10 or more outputs to said horizontal routing channel and said vertical routing channel.

27. (PREVIOUSLY ADDED) The programmable logic device

according to claim 26, wherein each of said first memory blocks comprises a first port connected to one of said horizontal routing channels and a second port connected to one of said vertical  
5 routing channels.

28. (PREVIOUSLY ADDED) The programmable logic device

according to claim 26, wherein each of said first memory blocks is configurable to a mode selected from the group consisting of (i) an asynchronous dual port memory mode, (ii) a synchronous dual port  
5 memory mode, and (iii) a synchronous FIFO memory mode.

29. (PREVIOUSLY ADDED) The programmable logic device of claim 26, wherein each of said logic block arrays comprises a plurality of programmably interconnected logic blocks, and each of said logic blocks comprises a plurality of macrocells.

30. (PREVIOUSLY ADDED) The programmable logic device of claim 26, comprising:

M number of horizontal routing channels;

N number of vertical routing channels;

5 N times M number of first memory blocks; and

N times M number of logic block arrays, wherein N plus M is greater than or equal to 2.

31. (PREVIOUSLY ADDED) The programmable logic device of claim 26, wherein each of said logic block arrays further comprises an interconnect matrix coupled to said horizontal routing channel and said vertical routing channel.

32. (PREVIOUSLY ADDED) The programmable logic device of claim 31, wherein each of said logic block arrays further comprises a second memory block coupled to said interconnect matrix.